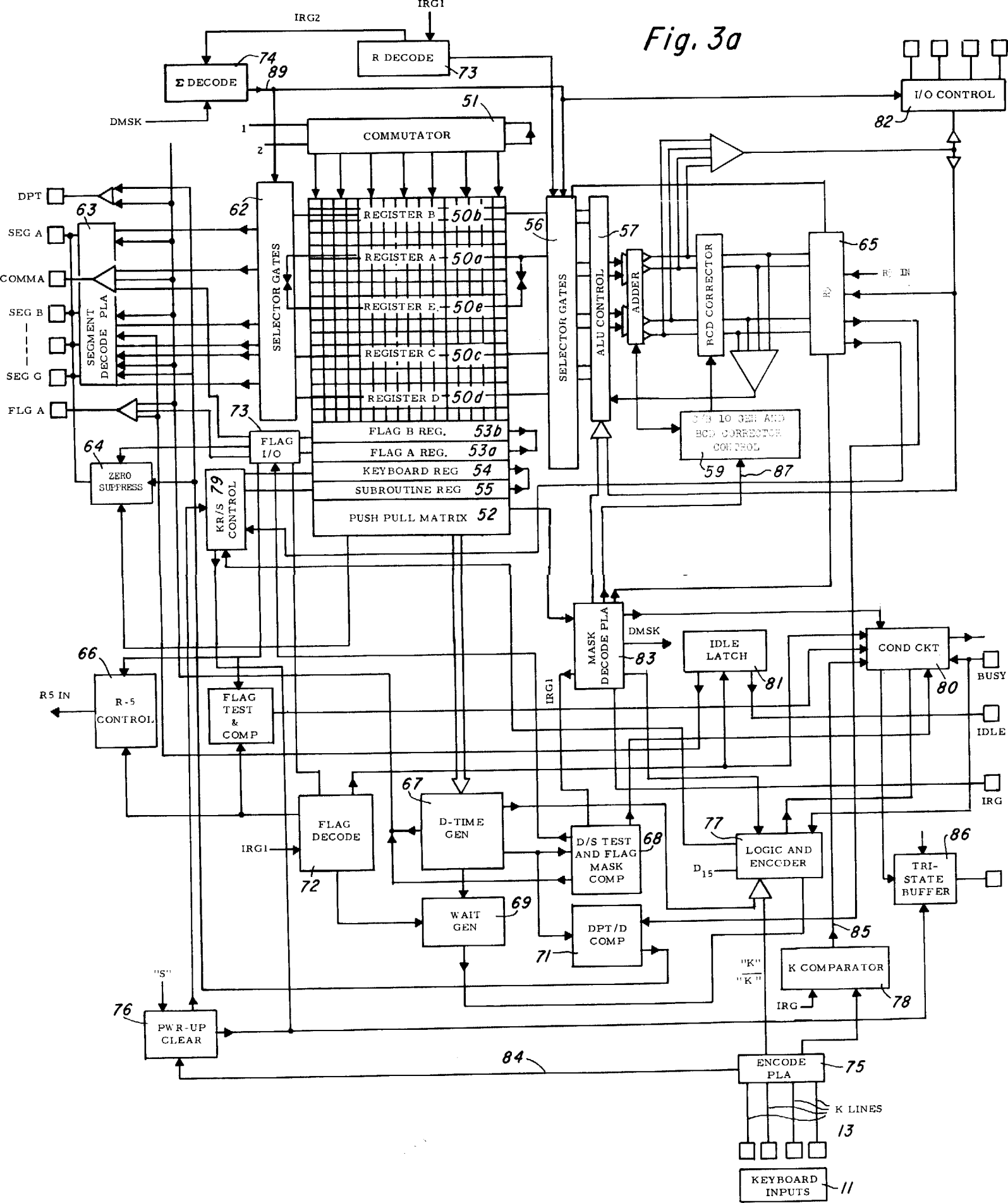

IRG2
IRG1
R DECODE
73
Σ DECODE
74
89
DMSK
I/O CONTROL
82
51
COMMUTATOR
1
2
DPT
SEG A
COMMA
SEG B
SEG G
FLG A
63
SEGMENT DECODE PLA
62
SELECTOR GATES
REGISTER B 50b
REGISTER A 50a
REGISTER E 50e
REGISTER C 50c
REGISTER D 50d
56
SELECTOR GATES
ALU CONTROL
57
ADDER
BCD CORRECTOR
65
R5 IN
73
FLAG I/O
FLAG B REG. 53b
FLAG A REG. 53a
KEYBOARD REG 54
SUBROUTINE REG 55
PUSH PULL MATRIX 52
64
ZERO SUPPRESS
KR/S CONTROL 79
59
87
MASK DECODE PLA
DMSK
83
IDLE LATCH
81
COND CKT
80
BUSY
IDLE
IRG
66
R5 IN
R-5 CONTROL
FLAG TEST & COMP
IRG1
67
FLAG DECODE
72
D-TIME GEN
D/S TEST AND FLAG MASK COMP
68
77
LOGIC AND ENCODER
D_{15}
86
TRI-STATE BUFFER
WAIT GEN
69
DPT/D COMP
71
85
K COMPARATOR
78
"K"
"K"
IRG
"S"
76
PWR-UP CLEAR
84
ENCODE PLA
75
K LINES
13
KEYBOARD INPUTS
11

Fig. 3a

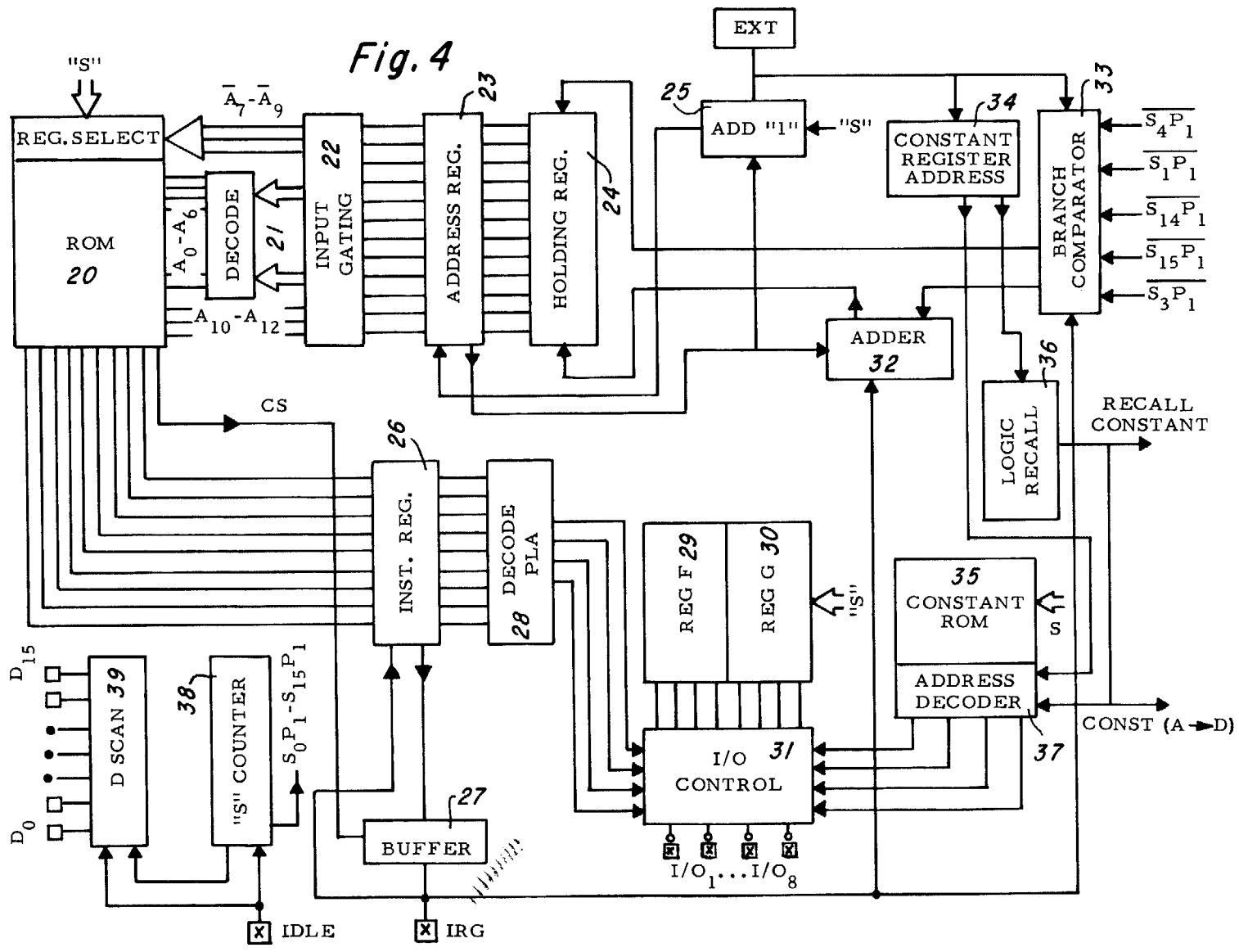


Fig. 4
"S"
REG. SELECT
ROM
20
$\overline{A}_7$-$\overline{A}_9$
A_0-A_6
DECODE
21
INPUT GATING
22
A_{10}-A_{12}
ADDRESS REG.
23
HOLDING REG.
24
EXT
25
ADD "1"
"S"
CONSTANT REGISTER ADDRESS
34
BRANCH COMPARATOR
33
$\overline{S_4P_1}$
$\overline{S_1P_1}$
$\overline{S_{14}P_1}$
$\overline{S_{15}P_1}$
$\overline{S_3P_1}$
ADDER
32
LOGIC RECALL
36
RECALL CONSTANT
CS
INST. REG.
26
DECODE PLA
28
REG F 29
REG G 30
"S"
35
CONSTANT ROM
S
ADDRESS DECODER
37
CONST (A→D)
I/O CONTROL
31
I/O_1...I/O_8
D_{15}
D_0
D SCAN 39
38
"S" COUNTER
S_0P_1-$S_{15}P_1$
BUFFER
27
IDLE
IRG

Fig. 8b1

Fig. 8b2

Fig. 8b3

Fig. 8b5

Fig. 8b6

Fig. 8b8

Fig. 8b10

Fig. 8c2

(SHEET 2)

Fig.8d1

Fig.8d3

Fig.8d6

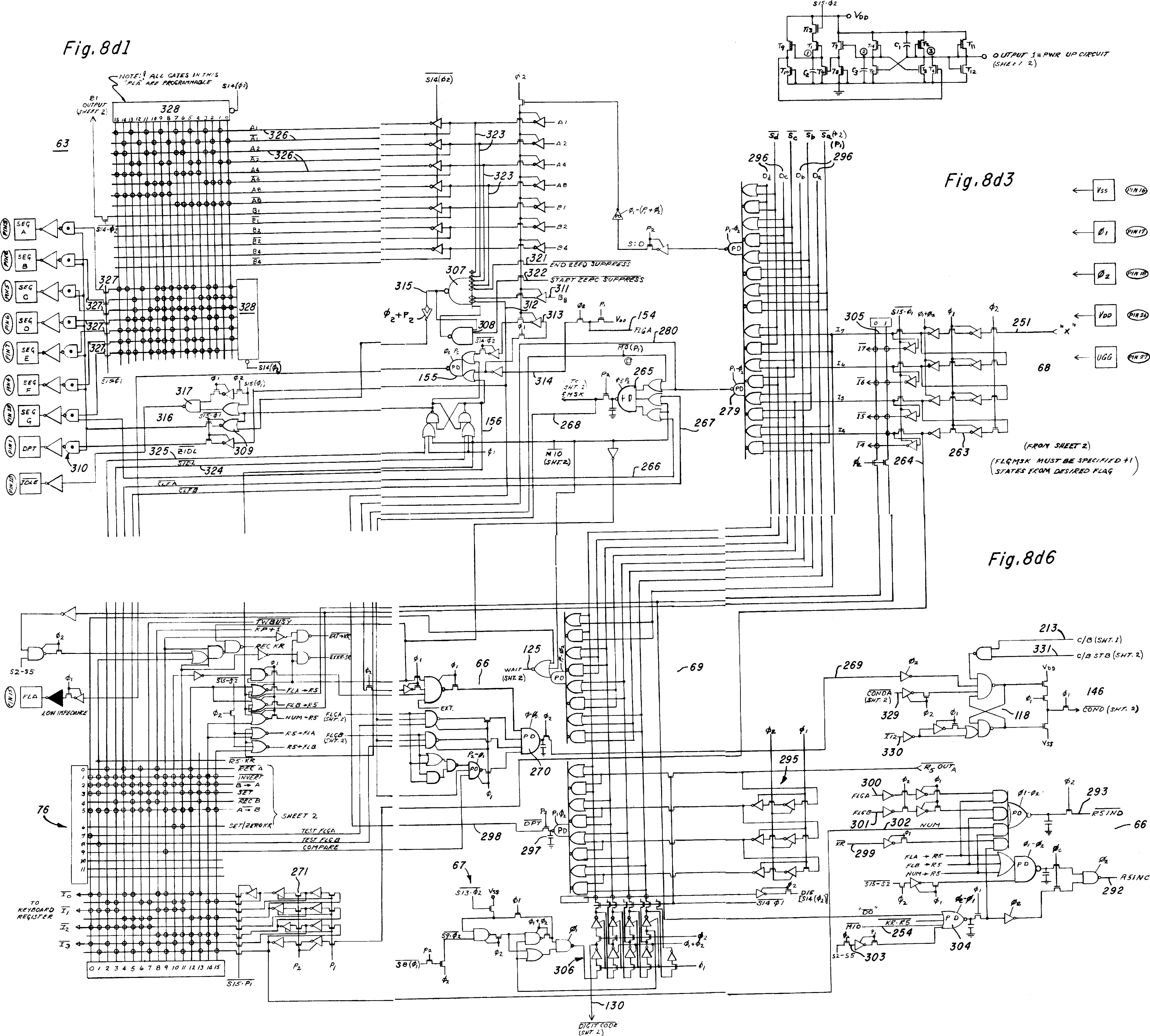


Fig. 9b1

Fig. 9b2

Fig. 9b3

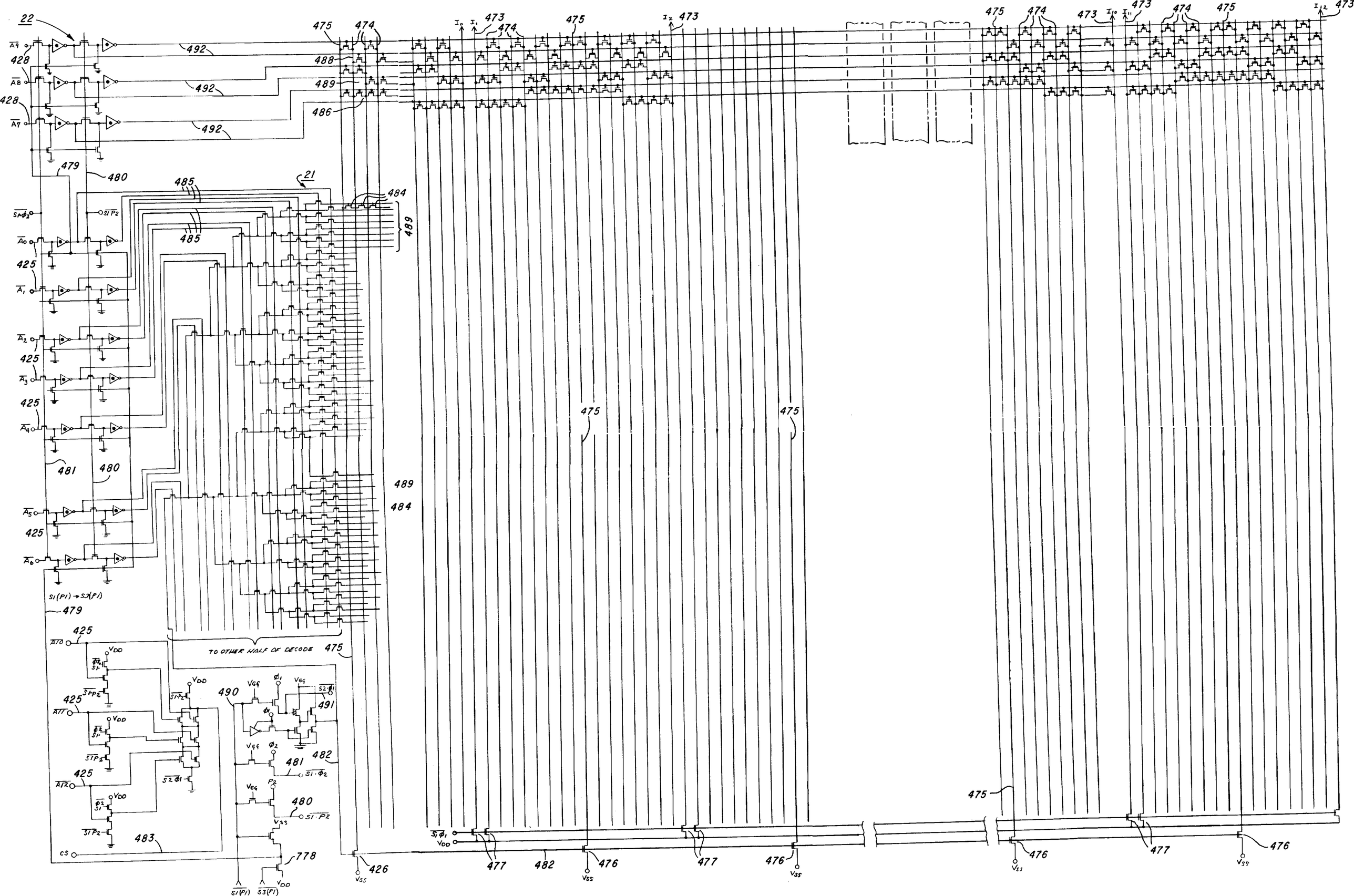
Fig. 9b4

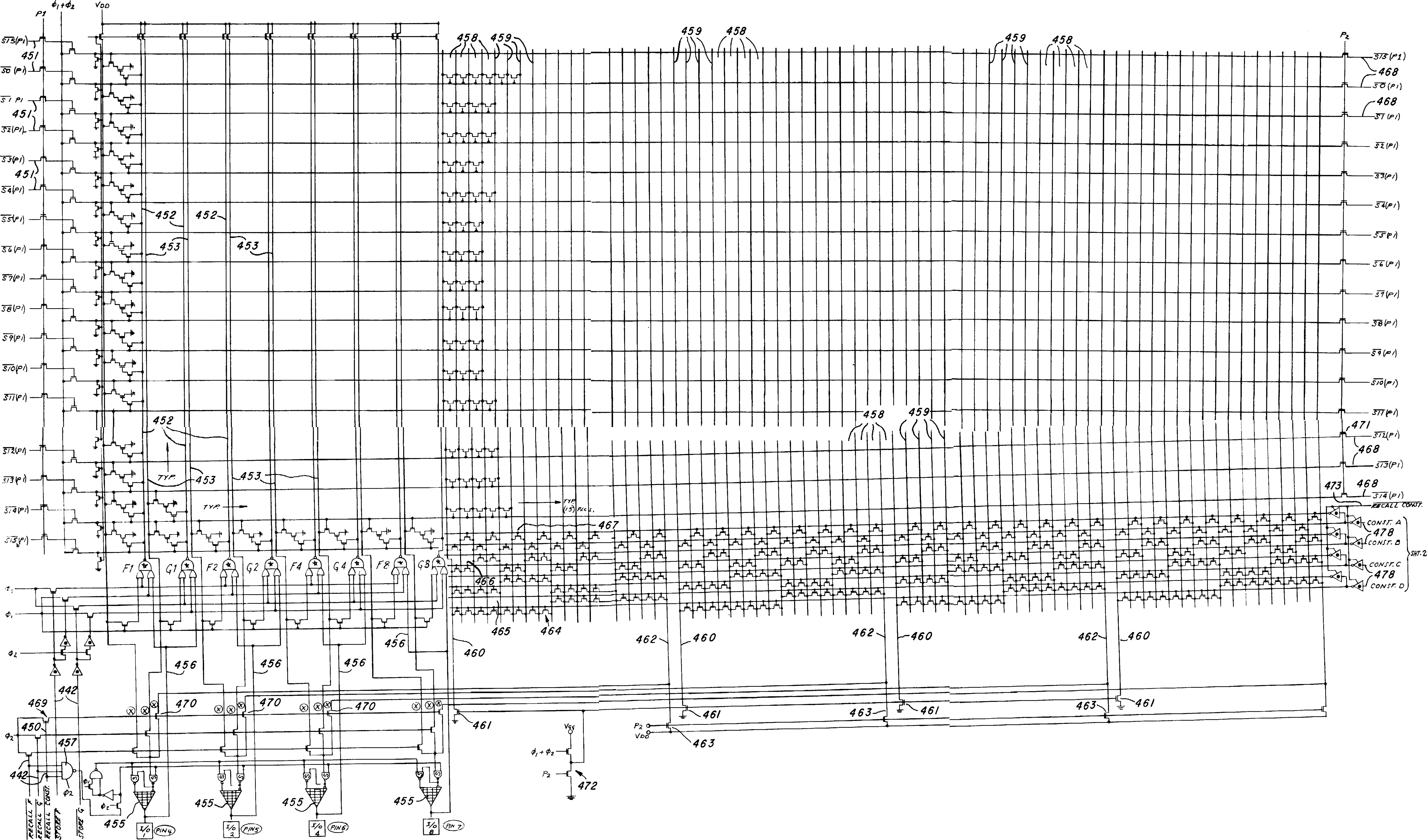
Fig. 9c1

Fig. 9c2

Fig. 9c3

Fig. 9c4


22
21
$\overline{A9}$
$\overline{A8}$
$\overline{A7}$
$\overline{A0}$
$\overline{A1}$
$\overline{A2}$
$\overline{A3}$
$\overline{A4}$
$\overline{A5}$
$\overline{A6}$
$\overline{A10}$
$\overline{A11}$
$\overline{A12}$
$\overline{S1\Phi_2}$
$\overline{S1P_2}$
$S1(P1) \rightarrow S3(P1)$
TO OTHER HALF OF DECODE
$\overline{S1\Phi_1}$
$\overline{S2\Phi_1}$
$\overline{S1\cdot\Phi_2}$
$\overline{S1\cdot P_2}$
V_{DD}
V_{SS}
V_{GG}
CS
$\overline{S1(P1)}$
$\overline{S3(P1)}$
I_0 I_1 I_2 I_{10} I_{11} I_{12}
425
428
475
474
473
476
477
479
480
481
482
483
484
485
486
488
489
490
491
492
778


P1
$\phi_1+\phi_2$
VDD
P2
451
452
453
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
478
F1
G1
F2
G2
F4
G4
F8
G8
TYP.
RECALL CONST.
CONST. A
CONST. B
CONST. C
CONST. D
SHT. 2
RECALL F
RECALL G
STORE F
STORE G
I/O 1
I/O 2
I/O 4
I/O 8
PIN 4
PIN 5
PIN 6
PIN 7
442
450